FORM PTO-1449 U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office	ATTY. DOCKET NO. 500.28166CX2	SERIAL NO. N t y t assigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	APPLICANT HOTTA, et al	
	FILING DATE May 14, 2001	GROUP 2152

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
Cu		4	7	2	2	0	5	0	1/88	Lee et al	395	375	
n		4	6	2	0	2	7	5	10/86	Wallach et al	395	800	
n		3	6	1	4	7	4	5	10/71	Podia et al	395	650	
Cu		4	9	2	8	2	2	6	5/90	Kamada et al	364	200	
u		3	7	7	1	1	3	8	11/73	Celtruda et al			
n		4	6	7	7	5	4	5	6/87	Blahut			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT YES	NO
n		0	1	4	9	0	4	9	7/85	EPO				
n		0	2	6	0	4	0	9	3/88	EPO				
n		8	8	0	9	0	3	5	11/88	WIPO				
n		0	0	8	2	9	0	3	7/83	EPO				
n		6	3	7	3	3	3	2	2/88	Japan				XX

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

v		Technical Summary, Multi-flow Computer, Inc., 4/30/87, pp/ 1-(3-7).
v		O. Serlin, "The Serlin Report on Parallel Processing", ITOM International Co., Issue No. 7, 12/87, pp. 10-18.
n		IEEE Journal of Solid-State Circuits, "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with on-chip Cache", Horowitz, et al, vol. sc-22, No. 5, October 1987, New York.
v		J. Bond, "Parallel Processing Concepts Finally come together in Real Systems", Computer Design, June 1, 1987, pp/ 51-74.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citati/n is considered, draw lin/through citation if n t in conformance and n t considered. Include copy of this form/with next c mmunication/to applicant

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✓		5	1	0	1	3	4	1	3/92	Circello et al	395	375	
✓		4	4	3	7	1	4	9	3/84	Pomerene et al			
✓		5	0	7	2	3	6	4	12/91	Jardine et al	395	375	5-24-89
✓		4	8	7	3	6	2	9	10/89	Harris et al			
✓		4	8	5	8	1	0	5	8/89	Kuriyama et al	395	375	3-26-87
✓		4	8	2	5	3	6	0	4/89	Knight, Jr.			
✓		4	7	8	9	9	2	5	12/88	Lahti	395	800	7-31-85
✓		5	0	4	3	8	6	8	8/91	Kitamura et al	395	775	12-24-87

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		DOCUMENT NUMBER						DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT YES	ABSTRACT NO
✓		4	5	9	2	3	2		12/91	EPO				
✓		3	2	8	8	2	4	6	12/91	Japan				XX
✓		4	5	5	9	6	6		11/91	EPO				
✓	6	3	1	3	1	2	3	0	6/88	Japan				

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✓		R. Acosta, et al, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors", IEEE Transactions on Computers vol. C-35, No. 9, Sept. 1986, pp. 815-828.
✓		D. Ditzel, et al "The Hardware Architecture of the Crisp Microprocessor" ACM, 0084-7495, pp. 309-319.
✓		Capozzi et al, "Non-sequential High-performance Processing", IBM Technical Disclosure Bulletin, vol. 27, No. 5, 10/84, pp. 2842-2844.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is c nsidered, draw line through citati n if not in conformance and not c nsidered. Include c py f this f rm with next c mmunicati n t applicant.

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✓		4	9	4	2	5	2	5	7/90	Shintani et al	395	Dig. 1	11/20/87
✓		5	2	8	7	4	6	5	2/94	Kurosawa et al			
✓		5	4	0	4	4	7	2	4/95	Kurosawa et al			
✓		5	5	6	1	7	7	5	10/96	Kurosawa et al			
✓		4	4	7	6	5	2	5	10/84	Ishii	364	Dig. 1	
✓		4	5	9	4	6	5	5	6/86	Hdo et al	364	DIG. 1	
✓		4	6	2	6	9	8	9	12/86	Rorii	395	375	
✓		4	6	4	4	4	6	6	2/87	Saito	395	725	
✓		4	7	9	4	5	1	7	12/88	Jones et al	395	725	
✓		4	9	1	6	6	0	6	4/90	Yamaoka et al	395	375	
✓		4	9	2	8	2	2	3	5/90	Dao et al	395	375	

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✓		0	1	4	7	8	5	8	7/85	EPO				
✓		0	0	4	2	4	4	2	12/81	EPO				
✓		0	2	3	9	0	8	1	9/87	EPO				
✓		0	1	0	1	5	9	6	8/83	EPO				

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✓		J. David, "Reducing the Branch Penalty in Pipelined Processors", Computer (July1988), pp. 47-55.
✓		Miller et al "Floating-Duplex Decode and Execution of Instruction", IBM Technical Disclosur Bulletin, vol. 23, No. 1, June 1980, pp. 409-412.
✓		G. Tjoden et al, "Detection and Parallel Execution of Independent Instructions", IEEE Transaction, vol. C-19, N . 10, Oct ber 1970, pp. 889-895.

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